LISTING OF CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1.   (Previously Presented) A computer-implemented method for tour planning, comprising:

creating a first schematic, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

creating a tour as an instance of the first schematic, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic;

determining whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier; and

in response, assigning the load to the first segment of the tour if it will produce a cost savings over the common carrier.

2.   (Canceled)

3.   (Original)   The method of claim 1, further comprising performing tour optimization on the tour.

4.   (Original)   The method of claim 1, wherein creating the first schematic further comprises creating the first schematic based on a load history.

5.   (Previously Presented)   The method of claim 1, wherein creating the first schematic further comprises creating the first schematic based on a forecast of loads.

6.   (Original)   The method of claim 1, wherein creating the tour further comprises creating the tour based on a plurality of loads in a load list.

7.   (Previously Presented)   A system for tour planning, comprising:

a memory; and

a microprocessor coupled to the memory and programmed to:

create a first schematic, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

create a tour as an instance of the first schematic, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic; and

determine whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier; and

in response, assign the load to the first segment of the tour if it will produce a cost savings over the common carrier.

8.   (Canceled)

9.   (Original)   The system of claim 7, wherein the microprocessor is further programmed to perform tour optimization on the tour.

10.   (Original)   The system of claim 7, wherein the microprocessor is further programmed to create the first schematic based on a load history.

11.   (Original)   The system of claim 7, wherein the microprocessor is further programmed to create the first schematic based on a forecast of loads.

12.   (Original)   The system of claim 7, wherein the microprocessor is further programmed to create the tour based on a plurality of loads in a load list.

13.   (Previously Presented) An article of manufacture containing instructions for tour planning, the instructions, when executed by a processor, causing the processor to perform stages comprising:

create a first schematic, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

create a tour as an instance of the first schematic, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic; and

determine whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier; and

in response, assign the load to the first segment of the tour if it will produce a cost savings over the common carrier.

14.   (Canceled)

15.   (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to perform tour optimization on the tour.

16.   (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the first schematic based on a load history.

17.   (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the first schematic based on a forecast of loads.

18.   (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the tour based on a plurality of loads in a load list.